Amendments to the Claims:

Please cancel claims 8-40.

This listing of claims will replace all prior versions, and listings, of the claims in the application:

Listing of Claims:

1. (Original) In the fabrication of a three dimensional memory where memory cells are formed at the intersection of generally parallel, spaced-apart rail-stacks disposed at a plurality of rail-stack levels, an improvement wherein the depth of etching in at least two etching steps used to form the rail-stacks in two adjacent rail-stack levels is approximately equal.

2. (Original) The improvement defined by claim 1, wherein each of the two etching steps etches a plurality of layers used to form the rail-stacks at one level of rail-stacks, and additionally partially etches rail-stacks in an underlying adjacent level of rail-stacks so as to form pillar structures in the underlying adjacent level of rail-stacks.

3. (Original) The improvement defined by claim 2, wherein the pillar structures comprise N- regions of silicon.

4. (Original) The improvement defined by claim 3, wherein the N- regions associated with diodes in the memory cells.

5. (Original) The improvement defined by claim 4, wherein the memory cells include an antifuse regions.

6. (Original) The improvement defined by claim 2, wherein the pillar structures are associated with diodes in the memory cells.

7. (Original) The improvement defined by claim 6, wherein the memory cells include antifuse regions.

8-40 (Canceled)